FORM PTO-1390 (REV. 5-93)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 10191/2197
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 10/030309

INTERNATIONAL APPLICATION NO. PCT/DE00/01812	INTERNATIONAL FILING DATE (03.06.00) 03 June 2000	PRIORITY DATE(S) CLAIMED (03.07.99) 03 July 1999

TITLE OF INVENTION
DIODE HAVING A METAL SEMICONDUCTOR CONTACT, AND METHOD FOR THE MANUFACTURE THEREOF

APPLICANT(S) FOR DO/EO/US

GOERLACH, Alfred

Applicant(s) herewith submit to the United States Designated/Elected Office (DO/EO/US) the following items and other information

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) immediately rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)) (unsigned).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A **FIRST** preliminary amendment.
    ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
14. ☒ A substitute specification and a marked up version thereof.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information: International Search Report, International Preliminary Examination Report and Form PCT/RO/101.

Express Mail No. EL244510250

JC13 Rec'd PCT/PTO 03 JAN 2002

U.S. APPLICATION NO. if known, see 37 C.F.R.1.5	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/030309	PCT/DE00/01812	10191/2197

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO $890.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) . . . $710.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $740.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $1,040.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	16 - 20 =	0	X $18.00	$ 0	
Independent Claims	2 - 3 =	0	X $84.00	$ 0	
Multiple dependent claim(s) (if applicable)			+ $280.00	$ 0	
TOTAL OF ABOVE CALCULATIONS =				$ 890	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				$	
SUBTOTAL =				$ 890	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$ 890	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$	
TOTAL FEES ENCLOSED =				$ 890	
				Amount to be: refunded	$
				charged	$

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 11-0600 in the amount of $890.00 to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 11-0600. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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(Reg. No. 42,194) for
SIGNATURE

Richard L. Mayer, Reg. No. 22,490
NAME

January 3, 2002
DATE

[10191/2197]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Alfred GOERLACH
Serial No.	:	To Be Assigned
Filed	:	Herewith
For	:	DIODE HAVING A METAL SEMICONDUCTOR CONTACT, AND METHOD FOR THE MANUFACTURE THEREOF
Art Unit	:	To Be Assigned
Examiner	:	To Be Assigned

Assistant Commissioner for Patents
P.O. Box 2327
Arlington, VA 22202

PRELIMINARY AMENDMENT AND
37 C.F.R. § 1.125 SUBSTITUTE SPECIFICATION STATEMENT

SIR:

Please amend without prejudice the above-identified application before examination, as set forth below.

IN THE SPECIFICATION AND ABSTRACT:

In accordance with 37 C.F.R. § 1.121(b)(3), a Substitute Specification (including the Abstract, but without claims) accompanies this response. It is respectfully requested that the Substitute Specification (including Abstract) be entered to replace the Specification of record.

IN THE CLAIMS:

On the first page of claims, first line, change "What is claimed is:" to --WHAT IS CLAIMED IS:--.

Please cancel, without prejudice, claims 1 to 16 in the underlying PCT application.

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Please add the following new claims:

--17. (New) A diode, comprising:

a semiconductor substrate arranged between a first metallic electrode and a second metallic electrode, the substrate highly doped in a first zone to form an ohmic transition to the first electrode and weakly doped in a second zone to form a rectifying transition to the second electrode;

wherein the first zone and the second zone are separated by a third zone of the semiconductor substrate doped more weakly than the second zone, the first zone, the second zone and the third zone having a same conductivity type, the second zone enclosed between the second electrode and the third zone.

18. (New) The diode according to claim 17, wherein a breakdown voltage between the second electrode and the third zone is at least three times as great as a breakdown voltage between the second electrode and the second zone.

19. (New) The diode according to claim 17, wherein the second zone is raised over a surface of the third zone, and the second electrode covers the second zone in a hat shape that includes a circumferential rim that touches the third zone.

20. (New) The diode according to claim 17, wherein the second zone is planar and island-type on a surface of the third zone, and the second electrode is flat and touches the third zone in an edge region.

21. (New) The diode according to claim 17, further comprising an insulating layer formed on a surface of the third zone surrounding the second zone, the edge of the second electrode touching the insulating layer.

22. (New) The diode according to claim 17, wherein at least one of the first electrode and the second electrode is applied to an oxide-free surface of the semiconductor substrate.

23. (New) The diode according to claim 17, wherein the semiconductor substrate includes one of Si and SiC.

24. (New) A method for manufacturing a diode, comprising the steps of:

producing, on a surface of a third zone of a semiconductor substrate that includes a strongly doped first zone, the third having weak doping, a second zone having stronger doping than the third zone, the first zone, the second zone and the third zone having a same conductivity type; and

depositing on the surface a first metallic electrode that encloses the second zone between itself and the third zone.

25. (New) The method according to claim 24, wherein the second zone is produced in the producing step on an overall surface of the third zone, the method further comprising the step of subsequently eroding the second zone locally to expose the third zone locally.

26. (New) The method according to claim 24, wherein the second zone is produced in the producing step be epitaxial layer growth.

27. (New) The method according to claim 25, wherein the eroding step includes the substep of sawing with a circular saw.

28. (New) The method according to claim 25, wherein the eroding step includes the substeps of masking and etching.

29. (New) The method according to claim 24, wherein the depositing step includes the substep of depositing the first electrode and a second metallic electrode by sputtering.

30. (New) The method according to claim 24, further comprising the step of sputtering before the depositing step make the surface of the semiconductor substrate oxide-free.

31. (New) The method according to claim 24, further comprising the step of heating the semiconductor substrate in an ultrahigh vacuum before the depositing step to free the surface of the semiconductor substrate of oxide.

32. (New) The method according to claim 24, further comprising the step of etching the semiconductor substrate before the depositing step.--.

REMARKS

This Preliminary Amendment cancels, without prejudice, claims 1 to 16 in the underlying PCT Application No. PCT/DE00/01812 and adds new claims 17 to 32. The new claims conform the claims to U.S. Patent and Trademark Office rules and do not add new matter to the application.

In accordance with 37 C.F.R. § 1.121(b)(3), the Substitute Specification (including the Abstract, but without the claims) contains no new matter. The amendments reflected in the Substitute Specification (including Abstract) are to conform the Specification and Abstract to U.S. Patent and Trademark Office rules or to correct informalities. As required by 37 C.F.R. § 1.121(b)(3)(iii) and § 1.125(b)(2), a Marked-Up Version of the Substitute Specification comparing the Specification of record and the Substitute Specification also accompanies this Preliminary Amendment. Approval and entry of the Substitute Specification (including Abstract) is respectfully requested.

The underlying PCT Application No. PCT/DE00/01812 includes an International Search Report, dated November 13, 2000. The Search Report includes a list of documents that were uncovered in the underlying PCT Application. A copy of the Search Report accompanies this Preliminary Amendment.

The underlying PCT Application No. PCT/DE00/01812 also includes an International Preliminary Examination Report, dated May 25, 2001. An English translation of the International Preliminary Examination Report accompanies this Preliminary Amendment.

Applicants assert that the subject matter of the present application is new, non-obvious, and useful. Prompt consideration and allowance of the application are respectfully requested.

Respectfully Submitted,

KENYON & KENYON

Dated: JANUARY 3, 2002

By: [signature] (Reg. No. 42,194) for
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DIODE HAVING A METAL SEMICONDUCTOR CONTACT, AND METHOD FOR THE MANUFACTURE THEREOF

FIELD OF THE INVENTION

The present invention relates to a diode having a semiconductor substrate that is situated between two metallic electrodes and that is strongly doped in a first zone in order to form an ohmic transition to the first electrode, and is weakly doped in a second zone having the same conductivity type in order to form a rectifying transition to the second electrode.

BACKGROUND INFORMATION

Semiconductor diodes of this type, also known as Schottky diodes, are conventional. They are distinguished by a small voltage drop in the conducting direction and a short turn-off time, because, in contrast to pn diodes or pin diodes, no minority charge carriers need be discharged in order to stop a flow of current.

Figure 4 illustrates a simple example embodiment of such a diode. Above a strongly doped zone 3 is arranegd a more weakly doped zone 1. A thin metal layer, made, for example, of aluminum, is applied to each of the two zones. The metal layer on the lower side of the substrate forms a first electrode 6, which is in ohmic contact with zone 3 of the semiconductor substrate arranged above it. The metal layer on the upper side of the semiconductor constitutes a second electrode 5 which forms, together with zone 1, a metal semiconductor contact having a diode characteristic. First electrode 6 represents the cathode, and second electrode 5 represents the anode of the diode.

If such a component is operated in the reverse direction, then, at a certain boundary voltage, a sharp increase in the

reverse current occurs as a result of avalanche multiplication, analogously to a one-sided abrupt pn transition. However, the boundary voltages, at which such an increase in the current occurs, are mostly significantly smaller than would be expected proportionately to the selected doping of zone 1. The deviation is typically of a factor of 3. The reason for this is that a rise in field strength occurs at the edges of electrodes 5, 6. For this reason, the avalanche multiplication begins at the edge of the component. The result is that diodes having the configuration illustrated in Figure 4 exhibit high reverse currents already below the breakdown voltage. In the case of an avalanche breakdown, high power losses occur at the diode edge, because the overall breakdown current is concentrated at this region. For this reason, diodes having the simple configuration illustrated in Figure 4 are not suitable for use as elements for limiting voltage.

A conventional solution to this problem is the configuration illustrated in Figure 5. This configuration is described, for example, in B. J. Baliga, Power Semiconductor Devices, PWS Publishing Company, Boston, U.S., 1995. An annular, circumferential p-doped layer 7 is additionally introduced into n-doped zone 1. In accordance with steps that are standard in planar technology, anode 5 is fashioned so that, on the one hand, it is contacted with n-doped second zone 1 and with p-doped layer 7, and that, on the other hand, the outer edge of anode 5 comes to rest on an oxide layer 8 on the surface of the semiconductor substrate. The circumferential p-doped layer 7 is called a guard ring. In this manner, a reduction in the edge field strength is achieved. The avalanche breakdown now no longer occurs at the edge, but rather is distributed in a uniform manner over the surface of second zone 1 inside guard ring 7. Because no local breakdowns occur at the edge at voltages below the desired breakdown boundary voltage, a Schottky diode having a guard ring can be used for voltage limitation.

The manufacture of such a diode is, however, associated with an increased expense. Thus, on the one hand, the manufacture of a flat, weakly doped zone such as zone 1 over a more strongly doped zone, such as zone 3, is expensive, because, in general, an epitaxial method must be used for this purpose. Subsequently, guard ring 7 must be structured and put in place, and oxide layer 8 must be structured, in order finally to enable anode 5 to be deposited thereupon in the desired form.

SUMMARY

In accordance with the present intention, a diode of the type indicated above is created that is suitable for use as a voltage limiter and may be manufactured easily and economically. These advantages are achieved due to the fact that, in the diode according to the present invention, the first and second zone are separated by a third zone of the semiconductor substrate, this third zone, having the same conductivity type as the two others, being doped more weakly than the second zone.

Through suitable choice of the dimensions and doping concentrations of the individual zones, it may be ensured that the breakdown voltage at the transition from the second electrode to the third zone is greater than to the more strongly doped second zone. As a result, when the breakdown voltage of this second zone is achieved, the edge field strength at an edge of the second electrode touching the third zone is smaller than in its region touching the second zone, so that an avalanche breakdown occurs only in the second zone.

The conventional guard ring, and the process steps required for its manufacture, may therefore be omitted. Since the diode requires only zones having the same conductivity type, a single doping agent is sufficient.

The dimensions and the dopings of the zones may be selected such that the (calculated) breakdown voltage in a contact region between the second electrode and the third zone is at least three times as great as that between the second electrode and the second zone.

According to a first example embodiment of the present invention, the second zone is raised over the surface of the third zone, and the second electrode covers the second zone in a hat shape, and has a surrounding rim that touches the second zone. Such a diode may be produced, for example, using a manufacturing process where, first, the second zone is produced on the overall surface of the third zone of the semiconductor substrate and is subsequently eroded locally, in order to expose the surface of the third zone locally.

This local erosion may include a sawing using a circular saw, or also a masking and etching method.

According to a second example embodiment of the present invention, the surface of the diode may also be planar, and the second zone may be embedded into the third zone in the manner of islands, and the second electrode is flat and touches the third zone in an edge region. Such a diode may be produced, for example, through the island-by-island application of a doping agent onto the surface of the semiconductor substrate, doped with the concentration of the third zone, and diffusing in of the doping agent.

In order to improve the contact between the electrodes and the semiconductor substrate, at least one of the electrodes may be applied to an oxide-free surface of the semiconductor substrate. In order to remove the oxide that is naturally present on a semiconductor crystal, a treatment of the surface through sputtering, through heating in an ultrahigh vacuum, or through suitable etching is possible. A sputter treatment, for example using argon ions, is in particular simple and useful

if the electrodes are subsequently also to be produced through the sputtering of metal onto the semiconductor substrate.

Additional features and advantages of the invention are derived from the following description of example embodiments, with reference to the Figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of the structure of an example embodiment of a diode according to the present invention.

Figure 2 is a cross-sectional view of the structure of another example embodiment of a diode according to the present invention.

Figure 3 is a cross-sectional view of the structure of a further example embodiment of a diode according to the present invention.

Figure 4 is a cross-sectional view a Schottky diode.

Figure 5 is a cross-sectional view of another Schottky diode.

DETAILED DESCRIPTION

In Figure 1, a diode according to the present invention is illustrated schematically in cross-section. A weakly doped (n^-) third semiconductor zone (as it is called) 2, having width W2, is arranged above a strongly n-doped (n^+) first semiconductor zone (as it is called) 3, having width W3. W3 may be smaller than W2. From the manufacturing standpoint, this arrangement may be advantageous because it enables the production of the first zone through the diffusing in of doping atoms from the surfaces into an n^-doped substrate, whereas the production of a weakly doped thin layer on a more strongly doped base may require the use of expensive epitaxial methods.

Located above zone 2 is a second zone (as it is called) 1 that is n-doped with medium strength (n), having width W1. Together with the thin metal layer of the anode 5, this zone represents the actual Schottky contact of the diode illustrated. Zone 1 is configured in its width and doping so that a desired reverse voltage UZ is achieved.

At all edges of the substrate, a recess 4 having depth T is cut in. This recess crosses second zone 1 and extends up to the weakly n-doped third zone 2. Anode 5 extends, in the shape of a hat, over the entire surface of zone 1 and its vertical lateral edges 9 in the region of recesses 4. The surface of third zone 2 exposed in recesses 4 is covered by rim 10 of the hat.

A metallization layer on the underside of second zone 3 forms a cathode 6 of the diode.

Width WR2, which is reduced in the area of recesses 4, and the doping of the weakly n-doped third zone 2, are selected such that a breakdown voltage UZR results for the direct transition between anode 5 and third zone 2 that is at least three times as large as breakdown voltage UZ of anode 5 to second zone 1. For this reason, as explained above, the field strength in the edge region, i.e., at rim 10 and in the area of lateral edges 9, is smaller than in the center of the anode, and the avalanche breakdown remains limited to second zone 1.

Since, moreover, in contrast to the case of a pn diode, the essential portion of the reverse current of a Schottky diode is determined by the barrier height (thermionic current), and, moreover, the barrier height depends on the reverse voltage (reduction of the barrier as a result of mirror charges), the reverse current at the edge of anode 5 at the transition to third zone 2 is, in fact, smaller than in the center region at second zone 1.

The diode illustrated in Figure 1 may be manufactured in the following manner. Beginning with a homogenous n^--doped semiconductor substrate, doping atoms are introduced into the layers of the substrate close to the surface. This introduction may, for example, occur through the occupation of the surfaces with the doping atoms and subsequent diffusing in, through which a concentration distribution having a Gauss profile is obtained, or else may occur through ion implantation. In this manner, one obtains a semiconductor substrate having two doped-on surface zones that correspond to the later zones 1 to 3 of the finished diode, and a center zone having an unchanged doping concentration corresponding to third zone 2.

In a subsequent step, the more weakly doped of the two surface zones is eroded locally until the third zone, the doping concentration of which has remained unchanged, is exposed. This local erosion may be performed, for example, with the aid of a circular saw, with which a multiplicity of grooves are cut into the surface of the substrate, between which island-type raised areas having a high degree of doping remain.

In order to improve the characteristics of the Schottky contact to be applied to this surface, an etching onto the semiconductor surface may follow the sawing. In this manner, the surface disturbed in its crystal structure by the sawing is eroded, and regions of the crystal that are located thereunder and that have remained undamaged are exposed.

The production of the recesses may also be effected using other methods, such as wet-chemical etching or gas-phase etching, with the use of a corresponding masking technique.

Before the depositing of electrodes 5 to 6, in addition, a suitable surface treatment of the substrate, for example etching in hydrofluoric acid (HF) or heating in an ultrahigh vacuum, may be performed, in order to remove the oxide that is

always naturally present on the substrate surface, and thus to create better surface characteristics for the Schottky contact.

Subsequently, the substrate is provided on both surfaces with a metal layer. For this purpose, a sputtering method may be used, because this allows a sputtering on, before the metal depositing, of the natural oxide layer in situ, for example using argon ions. Once the metal layers are deposited, the substrate is diced into individual components in the usual manner. For this purpose, as for the local erosion, a circular saw may be used, with which the substrate is cut apart in the center of each of the previously sawed-in recesses (dicing). The saw blade for dicing the substrate is significantly narrower than the saw blade used for sawing in recesses 4. Once the substrate is diced, one obtains the structure illustrated in cross-section in Figure 1.

As a concrete numerical example, the manufacture of a Schottky diode from silicon, having a limitation voltage of 48 volts, shall be considered. In a substrate having a homogenous doping of $1.8 \times 10^{15}/cm^3$ and a wafer thickness W1 + W2 + W3 of 120 μm, the doping materials are introduced into zones 1 (front side) and 3 (back side) by occupation and diffusion. In this manner, Gauss-shaped doping profiles are obtained in zones 1 and 3. For n-doped second zone 1, a surface concentration of $1.075 \times 10^{16}/cm^3$ is selected, and for the n^+-doped first zone 3, a surface concentration of $1 \times 10^{20}/cm^3$ is selected. In both cases, the diffusion length is 17 μm. Depth T of recess 4, which completely surrounds second zone 1, is 35 μm. The width of recess 4 before the sectioning of the individual components is approximately 100 μm. Electrodes 5 and 6 are each made of a solderable layer system having layers of Cr, NiV, and Ag, having respective layer thicknesses of approximately 80, 150, and 80 nanometers. In the separation of the diodes from one another, a narrow saw blade, having, for example, a width of

40 μm, is used, so that recess 4 and the surface of third zone 2 exposed therein and covered with metal remain present.

A surface on which island-type second zones 1 are separated by intervening regions of third zone 2 may also be achieved through a planar structuring. An example embodiment is illustrated in Figure 2. Here, n-doped second zone 1 and n^--doped third zone 2 have a common flat surface on which anode 5 covers the entire second zone 1 and, in its edge regions 11, a part of the surface of third zone 2. The manner of operation of this construction is the same as that illustrated in Figure 1. The doping profiles for zones 1 and 3 may be selected, as described above in connection with Figure 1. The width of the weakly doped zone may even be selected somewhat smaller (for a breakdown voltage UZ of 48 volts, W1 + W2 must be greater than 8 μm). It is important that anode 5 extend beyond the lateral diffusing out of second zone 1 in all directions, so that edge regions 11 form a ring that completely surrounds second zone 1 on the surface of third zone 2.

A third example embodiment of a Schottky diode according to the present invention is illustrated in Figure 3. It largely corresponds to the arrangement illustrated in Figure 2. In addition, another insulating layer 8, made, for example, of SiO_2, is present on the edge of the semiconductor substrate onto which the edge of anode 5 extends. For this reason, in this construction, in addition to the field strength reduction due to the high-ohmic third zone 2, at the edge there is also the effect of a magnetoresistor.

The diodes and manufacturing methods described herein, in particular those illustrated in Figure 1, are suitable for the manufacture of diodes using silicon, but in particular also using silicon carbide, as a semiconductor material. SiC diodes of this sort are of particular interest for use at high temperatures and high voltages (> 50 volts). At such voltages, conventional diodes made of silicon may be used only with

difficulty due to their high reverse currents and reverse losses. Here, silicon carbide is more suitable as a semiconductor material due to its low diffusion coefficients of doping atoms. However, at the same time, these low diffusion coefficients make the processing of this material more difficult, because they complicate or prevent a doping through application of a doping agent onto the surface of the semiconductor substrate and diffusing in thereof. For this reason, for the manufacture of a Schottky diode from silicon carbide having the structure illustrated in Figure 1, zones 2 and 1 are deposited on an SiC substrate epitaxially. The production of recesses 4 may occur, for example, by dry etching on the basis of gases containing fluorine.

ABSTRACT

A diode includes a semiconductor substrate that is arranged between two metallic electrodes, having a strongly doped first zone that forms an ohmic transition to the first electrode, a weakly doped second zone, having the same conductivity type, that forms a rectifying transition to the second electrode, and a third zone that, having the same conductivity type, is doped more weakly than the second zone. The third zone separates the first and the second zones from one another, and the second zone is enclosed between the second electrode and the third zone.

DIODE HAVING A METAL SEMICONDUCTOR CONTACT, AND METHOD FOR THE MANUFACTURE THEREOF

[Background Information

] **FIELD OF THE INVENTION**

The present invention [is directed] **relates** to a diode having a semiconductor substrate that is situated between two metallic electrodes and that is strongly doped in a first zone in order to form an ohmic transition to the first electrode, and is weakly doped in a second zone having the same conductivity type in order to form a rectifying transition to the second electrode.

BACKGROUND INFORMATION

Semiconductor diodes of this [sort] **type**, also known as Schottky diodes, [have long been known] **are conventional**. They are distinguished by a small voltage drop in the conducting direction and a short turn-off time, because, in contrast to pn diodes or pin diodes, no minority charge carriers need be discharged in order to stop a flow of current.

Figure 4 [shows] **illustrates** a simple [exemplary] **example** embodiment of such a diode. Above a strongly doped zone 3 is [situated] **arranegd** a more weakly doped zone 1. A thin metal layer, made, for example, of aluminum, is applied to each of the two zones. The metal layer on the lower side of the substrate forms a first electrode 6, which is in ohmic contact with zone 3 of the semiconductor substrate [situated] **arranged** above it. The metal layer on the upper side of the semiconductor constitutes a second electrode 5 which forms, together with zone 1, a metal semiconductor contact having a diode characteristic. First electrode 6 represents the cathode, and second electrode 5 **represents** the anode of the diode.

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If such a component is operated in the reverse direction, then, at a certain boundary voltage, a sharp increase in the reverse current occurs as a result of avalanche multiplication, analogously to a one-sided abrupt pn transition. However, the boundary voltages, at which such an increase in the current occurs, are mostly significantly smaller than would be expected proportionately to the selected doping of zone 1. The deviation is typically of a factor of 3. The reason for this is that a rise in field strength occurs at the edges of electrodes 5, 6. For this reason, the avalanche multiplication begins at the edge of the component. The result is that diodes having the [design shown] **configuration illustrated** in Figure [1] **4** exhibit high reverse currents already below the breakdown voltage. In the case of an avalanche breakdown, high power losses occur at the diode edge, because the overall breakdown current is concentrated at this region. For this reason, diodes having the simple [design shown] **configuration illustrated** in Figure **4** are not suitable for use as elements for limiting voltage.

A [known] **conventional** solution to this problem is the [design shown] **configuration illustrated** in Figure 5. This [design] **configuration** is [known] **described,** for example [from]**, in** B. J. Baliga, Power Semiconductor Devices, PWS Publishing Company, Boston, U.S., 1995. [Here, an] **An** annular, circumferential p-doped layer 7 is additionally introduced into n-doped zone 1. [With the aid of the] **In accordance with** steps that are standard in planar technology, anode 5 is [now] fashioned [in such a way] **so** that, on the one hand, it is contacted with n-doped second zone 1 and with p-doped layer 7, and that, on the other hand, the outer edge of anode 5 comes to rest on an oxide layer 8 on the surface of the semiconductor substrate. The circumferential p-doped layer 7 is called a guard ring. In this [way] **manner**, a reduction in the edge field strength is achieved. The avalanche breakdown

now no longer [takes place preferably] **occurs** at the edge, but rather is distributed in a uniform manner over the surface of second zone 1 inside guard ring 7. Because no local breakdowns occur at the edge at voltages below the desired breakdown boundary voltage, a Schottky diode having a guard ring can be used for voltage limitation.

The manufacture of such a diode is, however, associated with an increased expense. Thus, on the one hand, the manufacture of a flat, weakly doped zone such as zone 1 over a more strongly doped zone, such as zone 3, is expensive, because, in general, an epitaxial method must be used for this purpose. Subsequently, guard ring 7 must be structured and put in place, and oxide layer 8 must be structured, in order finally to enable anode 5 to be deposited thereupon in the desired form.

[Advantages of the Invention

] **SUMMARY**

[Through] **In accordance with** the present intention, a diode of the type indicated above is created that is suitable for use as a voltage limiter and may be manufactured easily and economically. These advantages are achieved due to the fact that, in the diode according to the present invention, the first and second zone are separated by a third zone of the semiconductor substrate, this third zone, having the same conductivity type as the two others, being doped more weakly than the second zone.

Through suitable choice of the dimensions and doping concentrations of the individual zones, it may be ensured that the breakdown voltage at the transition from the second electrode to the third zone is greater than to the more strongly doped second zone. As a result, when the breakdown voltage of this second zone is achieved, the edge field strength at an edge of the second electrode touching the third

zone is smaller than in its region touching the second zone, so that an avalanche breakdown [takes place] **occurs** only in the second zone.

The [known] **conventional** guard ring, and the process steps required for its manufacture, may therefore be omitted. Since the diode requires only zones having the same conductivity type, a single doping agent is sufficient.

[Preferably, the] **The** dimensions and the dopings of the zones [are] **may be** selected such that the (calculated) breakdown voltage in a contact region between the second electrode and the third zone is at least three times as great as that between the second electrode and the second zone.

According to a first [exemplary] **example** embodiment **of the present invention**, the second zone is raised over the surface of the third zone, and the second electrode covers the second zone in a hat shape, and has a surrounding rim that touches the second zone. Such a diode may be produced, for example, using a manufacturing process where, first, the second zone is produced on the overall surface of the third zone of the semiconductor substrate and is subsequently eroded locally, in order to expose the surface of the third zone locally.

This local erosion may include a sawing using a circular saw, or also a masking and etching method.

According to a second [design] **example embodiment of the present invention**, the surface of the diode may also be planar, and the second zone may be embedded into the third zone in the manner of islands, and the second electrode is flat and touches the third zone in an edge region. Such a diode may be produced, for example, through the island-by-island application of a doping agent onto the surface of the

semiconductor substrate, doped with the concentration of the third zone, and diffusing in of the doping agent.

In order to improve the contact between the electrodes and the semiconductor substrate, at least one of the electrodes [is preferably] **may be** applied to an oxide-free surface of the semiconductor substrate. In order to remove the oxide that is naturally present on a semiconductor crystal, a treatment of the surface through sputtering, through heating in an ultrahigh vacuum, or through suitable etching is possible. A sputter treatment, for example using argon ions, is in particular simple and useful if the electrodes are subsequently also to be produced through the sputtering of metal onto the semiconductor substrate.

Additional features and advantages of the invention are derived from the following description of [exemplary] **example** embodiments, with reference to the Figures.

[Figures 1, 2 and 3 each show structures of semiconductor diodes according to the present invention in cross-section, and

Figures 4 and 5, already discussed above, show analogous cross-sections of conventional Schottky diodes.]

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional view of the structure of an example embodiment of a diode according to the present invention.

Figure 2 is a cross-sectional view of the structure of another example embodiment of a diode according to the present invention.

Figure 3 is a cross-sectional view of the structure of a further example embodiment of a diode according to the present invention.

Figure 4 is a cross-sectional view a Schottky diode.

Figure 5 is a cross-sectional view of another Schottky diode.

[Description of the Exemplary Embodiments
] **DETAILED DESCRIPTION**

In Figure 1, a diode according to the present invention is [shown] **illustrated** schematically in cross-section. A weakly doped (n^-) third semiconductor zone (as it is called) 2, having width W2, is [situated] **arranged** above a strongly n-doped (n^+) first semiconductor zone (as it is called) 3, having width W3. [Here width] W3 [is preferably] **may be** smaller than W2. From the manufacturing standpoint, this [is] **arrangement may be** advantageous because it enables the production of the first zone through the diffusing in of doping atoms from the surfaces into an n^-doped substrate, whereas the production of a weakly doped thin layer on a more strongly doped base [would] **may** require the use of expensive epitaxial methods.

Located above zone 2 is a second zone (as it is called) 1 that is n-doped with medium strength (n), having width W1. Together with the thin metal layer of the anode 5, this zone represents the actual Schottky contact of the diode [shown] **illustrated**. Zone 1 is [designed] **configured** in its width and doping [in such a way] **so** that a desired reverse voltage UZ is achieved.

At all edges of the substrate, a recess 4 having depth T is cut in. This recess crosses second zone 1 and extends up to the weakly n-doped third zone 2. Anode 5 extends, in the shape of a hat, over the entire surface of zone 1 and its vertical lateral edges 9 in the region of recesses 4. The surface of third zone 2 exposed in recesses 4 is covered by rim 10 of the hat.

A metallization layer on the underside of second zone 3 forms a cathode 6 of the diode.

Width WR2, which is reduced in the area of recesses 4, and the doping of the weakly n-doped third zone 2, are selected such that a breakdown voltage UZR results for the direct transition between anode 5 and third zone 2 that is at least three times as large as breakdown voltage UZ of anode 5 to second zone 1. For this reason, as [already] explained **above**, the field strength in the edge region, i.e., at rim 10 and in the area of lateral edges 9, is smaller than in the center of the anode, and the avalanche breakdown remains limited to second zone 1.

Since, moreover, in contrast to the case of a pn diode, the essential portion of the reverse current of a Schottky diode is determined by the barrier height (thermionic current), and, moreover, the barrier height depends on the reverse voltage (reduction of the barrier as a result of mirror charges), the reverse current at the edge of anode 5 at the transition to third zone 2 is, in fact, smaller than in the center region at second zone 1.

The diode [shown] **illustrated** in [the figure] **Figure 1** may be manufactured in the following manner. Beginning with a homogenous n^--doped semiconductor substrate, doping atoms are introduced into the layers of the substrate close to the surface. This introduction may, for example, [take place]

occur through the occupation of the surfaces with the doping atoms and subsequent diffusing in, through which a concentration distribution having a Gauss profile is obtained, or else may [take place] **occur** through ion implantation. In this [way] **manner**, one obtains a semiconductor substrate having two doped-on surface zones that correspond to the later zones 1 to 3 of the finished diode, and a center zone having an unchanged doping concentration corresponding to third zone 2.

In a subsequent step, the more weakly doped of the two surface zones is eroded locally until the third zone, [whose] **the** doping concentration **of which** has remained unchanged, is exposed. This local erosion may be [carried out] **performed**, for example, with the aid of a circular saw, with which a multiplicity of grooves are cut into the surface of the substrate, between which island-type raised areas having a high degree of doping remain.

In order to improve the characteristics of the Schottky contact to be applied to this surface, an etching onto the semiconductor surface may follow the sawing. In this [way] **manner**, the surface disturbed in its crystal structure by the sawing is eroded, and regions of the crystal that are located thereunder and that have remained undamaged are exposed.

The production of the recesses may also be effected using other methods, such as wet-chemical etching or gas-phase etching, with the use of a corresponding masking technique.

Before the depositing of electrodes 5 to 6, in addition, a suitable surface treatment of the substrate, for example etching in hydrofluoric acid (HF) or heating in an ultrahigh vacuum, may be [carried out] **performed**, in order to remove the oxide that is always naturally present on the substrate

surface, and thus to create better surface characteristics for the Schottky contact.

Subsequently, the substrate is provided on both surfaces with a metal layer. For this purpose, a sputtering method [is preferably] **may be** used, because this allows a sputtering on, before the metal depositing, of the natural oxide layer in situ, for example using argon ions. Once the metal layers are deposited, the substrate is diced into individual components in the usual [fashion] **manner**. For this purpose, as for the local erosion, a circular saw [is preferably] **may be** used, with which the substrate is cut apart in the center of each of the previously sawed-in recesses (dicing). The saw blade for dicing the substrate is significantly narrower than the saw blade used for sawing in recesses 4. Once the substrate is diced, one obtains the structure [shown] **illustrated** in cross-section in Figure 1.

As a concrete numerical example, the manufacture of a Schottky diode from silicon, having a limitation voltage of 48 volts, shall be considered. In a substrate having a homogenous doping of $1.8 \times 10^{15}/cm^3$ and a wafer thickness W1 + W2 + W3 of 120 μm, the doping materials are introduced into zones 1 (front side) and 3 (back side) by occupation and diffusion. In this [way] **manner**, Gauss-shaped doping profiles are obtained in zones 1 and 3. For n-doped second zone 1, a surface concentration of $1.075 \times 10^{16}/cm^3$ is selected, and for the n^+-doped first zone 3, a surface concentration of $1 \times 10^{20}/cm^3$ is selected. In both cases, the diffusion length is 17 μm. Depth T of recess 4, which completely surrounds second zone 1, is 35 μm. The width of recess 4 before the sectioning of the individual components is approximately 100 μm. Electrodes 5 and 6 are each made of a solderable layer system having layers of Cr, NiV, and Ag, having respective layer thicknesses of approximately 80, 150, and 80 nanometers. In the separation of the diodes from one another, a narrow saw blade, having, for example, a width of

40 μm, is used, so that recess 4 and the surface of third zone 2 exposed therein and covered with metal remain present.

A surface on which island-type second zones 1 are separated by intervening regions of third zone 2 may also be achieved through a planar structuring. An [exemplary] **example** embodiment is [shown] **illustrated** in Figure 2. Here, n-doped second zone 1 and n^--doped third zone 2 have a common flat surface on which anode 5 covers the entire second zone 1 and, in its edge regions 11, a part of the surface of third zone 2. The manner of operation of this construction is the same as **that illustrated** in [the case of] Figure 1. The doping profiles for zones 1 and 3 may be selected, as **described** above[,] in connection with Figure 1. The width of the weakly doped zone may [here] even be selected somewhat smaller (for a breakdown voltage UZ of 48 volts, W1 + W2 must be greater than 8 μm). It is important that anode 5 extend beyond the lateral diffusing out of second zone 1 in all directions, so that edge regions 11 form a ring that completely surrounds second zone 1 on the surface of third zone 2.

A third example **embodiment** of a Schottky diode according to the present invention is [shown] **illustrated** in Figure 3. It largely corresponds to the [design shown] **arrangement illustrated** in Figure 2[; in]**. In** addition, another insulating layer 8, made, for example, of SiO_2, is present on the edge of the semiconductor substrate onto which the edge of anode 5 extends. For this reason, in this construction, in addition to the field strength reduction due to the high-ohmic third zone 2, at the edge there is also the effect of a magnetoresistor.

The diodes and manufacturing methods described [here] **herein**, in particular those [according to] **illustrated in** Figure 1, are suitable for the manufacture of diodes using silicon, but in particular also using silicon carbide, as a semiconductor

material. SiC diodes of this sort are of particular interest for use at high temperatures and high voltages (> 50 volts). At such voltages, conventional diodes made of silicon may be used only with difficulty due to their high reverse currents and reverse losses. Here, silicon carbide is more suitable as a semiconductor material due to its low diffusion coefficients of doping atoms. However, at the same time, these low diffusion coefficients make the processing of this material more difficult, because they complicate or prevent a doping through application of a doping agent onto the surface of the semiconductor substrate and diffusing in thereof. For this reason, for the manufacture of a Schottky diode from silicon carbide having the structure [shown] **illustrated** in Figure 1, zones 2 and 1 are deposited on an SiC substrate epitaxially. [Here, the] **The** production of recesses 4 may [take place] **occur**, for example, by dry etching on the basis of gases containing fluorine.

[Abstract

] **ABSTRACT**

A diode includes a semiconductor substrate that is [situated] **arranged** between two metallic electrodes [(5,6)], having a strongly doped first zone [(3)] that forms an ohmic transition to the first electrode [(6)], a weakly doped second zone [(1)], having the same conductivity type, that forms a rectifying transition to the second electrode [(5)], and a third zone [(2)] that, having the same conductivity type, is doped more weakly than the second zone [(3); the]**. The** third zone [(2)] separates the first and the second zones [(1,3)] from one another, and the second zone [(1)] is enclosed between the second electrode [(5)] and the third zone [(2)].

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DIODE HAVING A METAL SEMICONDUCTOR CONTACT, AND METHOD FOR THE MANUFACTURE THEREOF

Background Information

The present invention is directed to a diode having a semiconductor substrate that is situated between two metallic electrodes and that is strongly doped in a first zone in order to form an ohmic transition to the first electrode, and is weakly doped in a second zone having the same conductivity type in order to form a rectifying transition to the second electrode. Semiconductor diodes of this sort, also known as Schottky diodes, have long been known. They are distinguished by a small voltage drop in the conducting direction and a short turn-off time, because, in contrast to pn diodes or pin diodes, no minority charge carriers need be discharged in order to stop a flow of current.

Figure 4 shows a simple exemplary embodiment of such a diode. Above a strongly doped zone 3 is situated a more weakly doped zone 1. A thin metal layer, made for example of aluminum, is applied to each of the two zones. The metal layer on the lower side of the substrate forms a first electrode 6 which is in ohmic contact with zone 3 of the semiconductor substrate situated above it. The metal layer on the upper side of the semiconductor constitutes a second electrode 5 which forms, together with zone 1, a metal semiconductor contact having a diode characteristic. First electrode 6 represents the cathode, and second electrode 5 the anode of the diode.

If such a component is operated in the reverse direction, then, at a certain boundary voltage, a sharp increase in the reverse current occurs as a result of avalanche multiplication, analogously to a one-sided abrupt pn transition. However, the boundary voltages, at which such an

increase in the current occurs, are mostly significantly smaller than would be expected proportionately to the selected doping of zone 1. The deviation is typically of a factor of 3. The reason for this is that a rise in field strength occurs at the edges of electrodes 5, 6. For this reason, the avalanche multiplication begins at the edge of the component. The result is that diodes having the design shown in Figure 1 exhibit high reverse currents already below the breakdown voltage. In the case of an avalanche breakdown, high power losses occur at the diode edge, because the overall breakdown current is concentrated at this region. For this reason, diodes having the simple design shown in Figure are not suitable for use as elements for limiting voltage.

A known solution to this problem is the design shown in Figure 5. This design is known for example from B. J. Baliga, Power Semiconductor Devices, PWS Publishing Company, Boston, U.S., 1995. Here, an annular, circumferential p-doped layer 7 is additionally introduced into n-doped zone 1. With the aid of the steps that are standard in planar technology, anode 5 is now fashioned in such a way that, on the one hand, it is contacted with n-doped second zone 1 and with p-doped layer 7, and that, on the other hand, the outer edge of anode 5 comes to rest on an oxide layer 8 on the surface of the semiconductor substrate. The circumferential p-doped layer 7 is called a guard ring. In this way, a reduction in the edge field strength is achieved. The avalanche breakdown now no longer takes place preferably at the edge, but rather is distributed in a uniform manner over the surface of second zone 1 inside guard ring 7. Because no local breakdowns occur at the edge at voltages below the desired breakdown boundary voltage, a Schottky diode having a guard ring can be used for voltage limitation.

The manufacture of such a diode is, however, associated with an increased expense. Thus, on the one hand, the manufacture of a flat, weakly doped zone such as zone 1 over a more

strongly doped zone, such as zone 3, is expensive, because, in general, an epitaxial method must be used for this purpose. Subsequently, guard ring 7 must be structured and put in place, and oxide layer 8 must be structured, in order finally to enable anode 5 to be deposited thereupon in the desired form.

Advantages of the Invention

Through the present intention, a diode of the type indicated above is created that is suitable for use as a voltage limiter and may be manufactured easily and economically. These advantages are achieved due to the fact that, in the diode according to the present invention, the first and second zone are separated by a third zone of the semiconductor substrate, this third zone, having the same conductivity type as the two others, being doped more weakly than the second zone.

Through suitable choice of the dimensions and doping concentrations of the individual zones, it may be ensured that the breakdown voltage at the transition from the second electrode to the third zone is greater than to the more strongly doped second zone. As a result, when the breakdown voltage of this second zone is achieved, the edge field strength at an edge of the second electrode touching the third zone is smaller than in its region touching the second zone, so that an avalanche breakdown takes place only in the second zone.

The known guard ring, and the process steps required for its manufacture, may therefore be omitted. Since the diode requires only zones having the same conductivity type, a single doping agent is sufficient.

Preferably, the dimensions and the dopings of the zones are selected such that the (calculated) breakdown voltage in a contact region between the second electrode and the third zone

is at least three times as great as that between the second electrode and the second zone.

According to a first exemplary embodiment, the second zone is raised over the surface of the third zone, and the second electrode covers the second zone in a hat shape, and has a surrounding rim that touches the second zone. Such a diode may be produced, for example, using a manufacturing process where, first, the second zone is produced on the overall surface of the third zone of the semiconductor substrate and is subsequently eroded locally, in order to expose the surface of the third zone locally.

This local erosion may include a sawing using a circular saw, or also a masking and etching method.

According to a second design, the surface of the diode may also be planar, and the second zone may be embedded into the third zone in the manner of islands, and the second electrode is flat and touches the third zone in an edge region. Such a diode may be produced, for example, through the island-by-island application of a doping agent onto the surface of the semiconductor substrate, doped with the concentration of the third zone, and diffusing in of the doping agent.

In order to improve the contact between the electrodes and the semiconductor substrate, at least one of the electrodes is preferably applied to an oxide-free surface of the semiconductor substrate. In order to remove the oxide that is naturally present on a semiconductor crystal, a treatment of the surface through sputtering, through heating in an ultrahigh vacuum, or through suitable etching is possible. A sputter treatment, for example using argon ions, is in particular simple and useful if the electrodes are subsequently also to be produced through the sputtering of metal onto the semiconductor substrate.

Additional features and advantages of the invention are derived from the following description of exemplary embodiments, with reference to the Figures.

Figures 1, 2 and 3 each show structures of semiconductor diodes according to the present invention in cross-section, and

Figures 4 and 5, already discussed above, show analogous cross-sections of conventional Schottky diodes.

Description of the Exemplary Embodiments

In Figure 1, a diode according to the present invention is shown schematically in cross-section. A weakly doped (n^-) third semiconductor zone (as it is called) 2, having width W2, is situated above a strongly n-doped (n^+) first semiconductor zone (as it is called) 3, having width W3. Here width W3 is preferably smaller than W2. From the manufacturing standpoint, this is advantageous because it enables the production of the first zone through the diffusing in of doping atoms from the surfaces into an n^-doped substrate, whereas the production of a weakly doped thin layer on a more strongly doped base would require the use of expensive epitaxial methods.

Located above zone 2 is a second zone (as it is called) 1 that is n-doped with medium strength (n), having width W1. Together with the thin metal layer of the anode 5, this zone represents the actual Schottky contact of the diode shown. Zone 1 is designed in its width and doping in such a way that a desired reverse voltage UZ is achieved.

At all edges of the substrate, a recess 4 having depth T is cut in. This recess crosses second zone 1 and extends up to the weakly n-doped third zone 2. Anode 5 extends, in the shape

of a hat, over the entire surface of zone 1 and its vertical lateral edges 9 in the region of recesses 4. The surface of third zone 2 exposed in recesses 4 is covered by rim 10 of the hat.

A metallization layer on the underside of second zone 3 forms a cathode 6 of the diode.

Width WR2, which is reduced in the area of recesses 4, and the doping of the weakly n-doped third zone 2, are selected such that a breakdown voltage UZR results for the direct transition between anode 5 and third zone 2 that is at least three times as large as breakdown voltage UZ of anode 5 to second zone 1. For this reason, as already explained, the field strength in the edge region, i.e., at rim 10 and in the area of lateral edges 9, is smaller than in the center of the anode, and the avalanche breakdown remains limited to second zone 1.

Since, moreover, in contrast to the case of a pn diode, the essential portion of the reverse current of a Schottky diode is determined by the barrier height (thermionic current), and, moreover, the barrier height depends on the reverse voltage (reduction of the barrier as a result of mirror charges), the reverse current at the edge of anode 5 at the transition to third zone 2 is, in fact, smaller than in the center region at second zone 1.

The diode shown in the figure may be manufactured in the following manner. Beginning with a homogenous n^--doped semiconductor substrate, doping atoms are introduced into the layers of the substrate close to the surface. This introduction may, for example, take place through the occupation of the surfaces with the doping atoms and subsequent diffusing in, through which a concentration distribution having a Gauss profile is obtained, or else may take place through ion implantation. In this way, one obtains a semiconductor substrate having two doped-on surface zones

that correspond to the later zones 1 to 3 of the finished diode, and a center zone having an unchanged doping concentration corresponding to third zone 2.

In a subsequent step, the more weakly doped of the two surface zones is eroded locally until the third zone, whose doping concentration has remained unchanged, is exposed. This local erosion may be carried out, for example, with the aid of a circular saw, with which a multiplicity of grooves are cut into the surface of the substrate, between which island-type raised areas having a high degree of doping remain.

In order to improve the characteristics of the Schottky contact to be applied to this surface, an etching onto the semiconductor surface may follow the sawing. In this way, the surface disturbed in its crystal structure by the sawing is eroded, and regions of the crystal that are located thereunder and that have remained undamaged are exposed.

The production of the recesses may also be effected using other methods, such as wet-chemical etching or gas-phase etching, with the use of a corresponding masking technique.

Before the depositing of electrodes 5 to 6, in addition, a suitable surface treatment of the substrate, for example etching in hydrofluoric acid (HF) or heating in an ultrahigh vacuum, may be carried out, in order to remove the oxide that is always naturally present on the substrate surface, and thus to create better surface characteristics for the Schottky contact.

Subsequently, the substrate is provided on both surfaces with a metal layer. For this purpose, a sputtering method is preferably used, because this allows a sputtering on, before the metal depositing, of the natural oxide layer in situ, for example using argon ions. Once the metal layers are deposited, the substrate is diced into individual components in the usual

fashion. For this purpose, as for the local erosion, a circular saw is preferably used, with which the substrate is cut apart in the center of each of the previously sawed-in recesses (dicing). The saw blade for dicing the substrate is significantly narrower than the saw blade used for sawing in recesses 4. Once the substrate is diced, one obtains the structure shown in cross-section in Figure 1.

As a concrete numerical example, the manufacture of a Schottky diode from silicon, having a limitation voltage of 48 volts, shall be considered. In a substrate having a homogenous doping of $1.8 \times 10^{15}/cm^3$ and a wafer thickness W1 + W2 + W3 of 120 μm, the doping materials are introduced into zones 1 (front side) and 3 (back side) by occupation and diffusion. In this way, Gauss-shaped doping profiles are obtained in zones 1 and 3. For n-doped second zone 1, a surface concentration of $1.075 \times 10^{16}/cm^3$ is selected, and for the n^+-doped first zone 3, a surface concentration of $1 \times 10^{20}/cm^3$ is selected. In both cases, the diffusion length is 17 μm. Depth T of recess 4, which completely surrounds second zone 1, is 35 μm. The width of recess 4 before the sectioning of the individual components is approximately 100 μm. Electrodes 5 and 6 are each made of a solderable layer system having layers of Cr, NiV, and Ag, having respective layer thicknesses of approximately 80, 150, and 80 nanometers. In the separation of the diodes from one another, a narrow saw blade, having, for example, a width of 40 μm, is used, so that recess 4 and the surface of third zone 2 exposed therein and covered with metal remain present.

A surface on which island-type second zones 1 are separated by intervening regions of third zone 2 may also be achieved through a planar structuring. An exemplary embodiment is shown in Figure 2. Here, n-doped second zone 1 and n^--doped third zone 2 have a common flat surface on which anode 5 covers the entire second zone 1 and, in its edge regions 11, a part of the surface of third zone 2. The manner of operation of this construction is the same as in the case of Figure 1. The

doping profiles for zones 1 and 3 may be selected, as above, in connection with Figure 1. The width of the weakly doped zone may here even be selected somewhat smaller (for a breakdown voltage UZ of 48 volts, W1 + W2 must be greater than 8 μm). It is important that anode 5 extend beyond the lateral diffusing out of second zone 1 in all directions, so that edge regions 11 form a ring that completely surrounds second zone 1 on the surface of third zone 2.

A third example of a Schottky diode according to the present invention is shown in Figure 3. It largely corresponds to the design shown in Figure 2; in addition, another insulating layer 8, made for example of SiO_2, is present on the edge of the semiconductor substrate onto which the edge of anode 5 extends. For this reason, in this construction, in addition to the field strength reduction due to the high-ohmic third zone 2, at the edge there is also the effect of a magnetoresistor.

The diodes and manufacturing methods described here, in particular those according to Figure 1, are suitable for the manufacture of diodes using silicon, but in particular also using silicon carbide, as a semiconductor material. SiC diodes of this sort are of particular interest for use at high temperatures and high voltages (> 50 volts). At such voltages, conventional diodes made of silicon may be used only with difficulty due to their high reverse currents and reverse losses. Here, silicon carbide is more suitable as a semiconductor material due to its low diffusion coefficients of doping atoms. However, at the same time, these low diffusion coefficients make the processing of this material more difficult, because they complicate or prevent a doping through application of a doping agent onto the surface of the semiconductor substrate and diffusing in thereof. For this reason, for the manufacture of a Schottky diode from silicon carbide having the structure shown in Figure 1, zones 2 and 1 are deposited on an SiC substrate epitaxially. Here, the production of recesses 4 may take place, for example, by dry

etching on the basis of gases containing fluorine.

What is claimed is:

1. A diode having a semiconductor substrate situated between two metallic electrodes (5,6), the substrate being highly doped in a first zone (3) in order to form an ohmic transition to the first electrode (6), and being weakly doped in a second zone (1) having the same conductivity type, in order to form a rectifying transition to the second electrode (5), wherein both zones (1,3) are separated by a third zone (2) of the semiconductor substrate, the third zone, having the same conductivity type, being doped more weakly than the second zone (1), and the second zone (1) is enclosed between the second electrode (5) and the third zone (2).

2. The diode according to Claim 1, wherein the breakdown voltage between the second electrode (5) and the third zone (2) is at least three times as great as that between the second electrode (5) and the second zone (1).

3. The diode according to Claim 1 or 2, wherein the second zone (1) is raised over the surface of the third zone (2), and the second electrode (5) covers the second zone (1) in the manner of a hat, and has a circumferential rim (10) that touches the third zone (2).

4. The diode according to Claim 1 or 2, wherein the second zone (1) is fashioned in planar and island-type fashion on the surface of the third zone (2), and the second electrode (5) is flat and touches the third zone (2) in an edge region (11).

5. The diode according to one of the preceding claims, wherein an insulating layer (8) is formed on the surface of the third zone (2) surrounding the second zone (1), and the edge of the second electrode (5) touches the insulating layer (8).

6. The diode according to one of the preceding claims, wherein at least one of the electrodes (5,6) is applied to an oxide-

free surface of the semiconductor substrate.

7. The diode according to one of the preceding claims, wherein the semiconductor substrate is Si or SiC.

8. A method for manufacturing a diode, in particular according to one of the preceding claims, wherein, on a surface of a third zone (2) of a semiconductor substrate that includes a strongly doped first zone (3) and the third zone (2) having weak doping and the same conductivity type, a second zone (1) having the same conductivity type and having stronger doping than that of the third zone (2) is produced, and, on the surface, a metallic electrode (5) is deposited that encloses the second zone (1) between itself and the third zone (2).

9. The method according to Claim 8, wherein the second zone (1) is produced on the overall surface of the third zone (2), and is subsequently eroded locally in order again to expose the third zone (2) locally.

10. The method according to Claim 8, wherein the second zone (1) is produced through epitaxial layer growth.

11. The method according to Claim 9 or 10, wherein the local erosion includes a sawing using a circular saw.

12. The method according to Claim 9 or 10, wherein the local erosion includes a masking and etching.

13. The method according to one of Claims 8 through 12, wherein the electrodes (5,6) are deposited through sputtering.

14. The method according to one of Claims 8 through 13, wherein the surface of the semiconductor substrate is made oxide-free through sputtering before the depositing of the electrodes (5,6).

15. The method according to one of Claims 8 through 14, wherein the semiconductor substrate is heated in an ultrahigh vacuum before the depositing of the electrodes (5,6) in order to free its surface of oxide.

16. The method according to one of Claims 8 through 15, wherein the semiconductor substrate is etched before the depositing of the electrodes (5,6).

Abstract

A diode includes a semiconductor substrate that is situated between two metallic electrodes (5,6), having a strongly doped first zone (3) that forms an ohmic transition to the first electrode (6), a weakly doped second zone (1), having the same conductivity type, that forms a rectifying transition to the second electrode (5), and a third zone (2) that, having the same conductivity type, is doped more weakly than the second zone (3); the third zone (2) separates the first and the second zones (1,3) from one another, and the second zone (1) is enclosed between the second electrode (5) and the third zone (2).

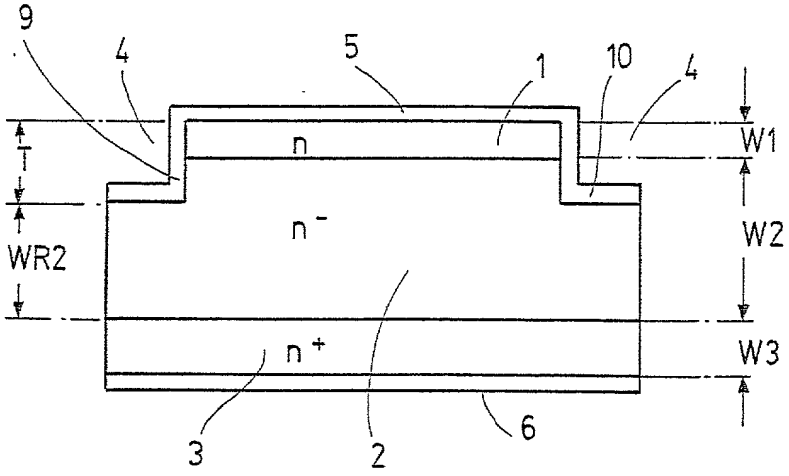

Fig. 1

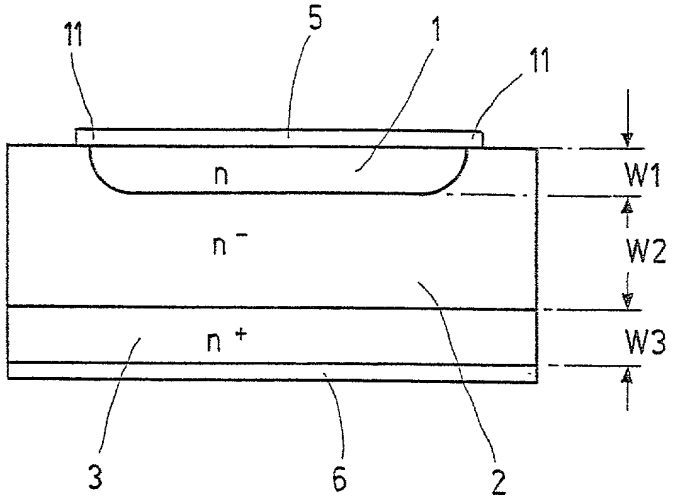

Fig. 2

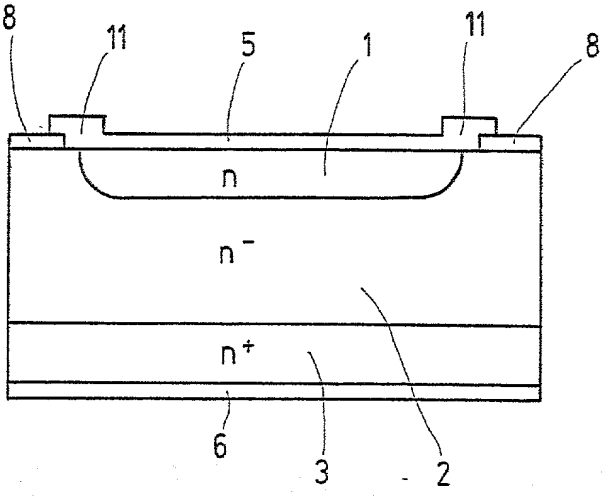

Fig. 3

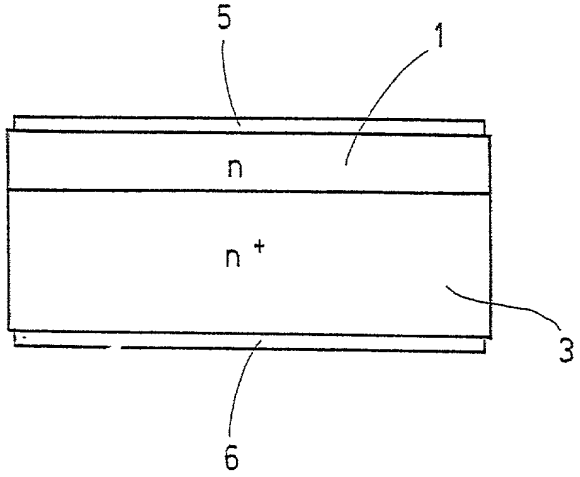

Fig. 4

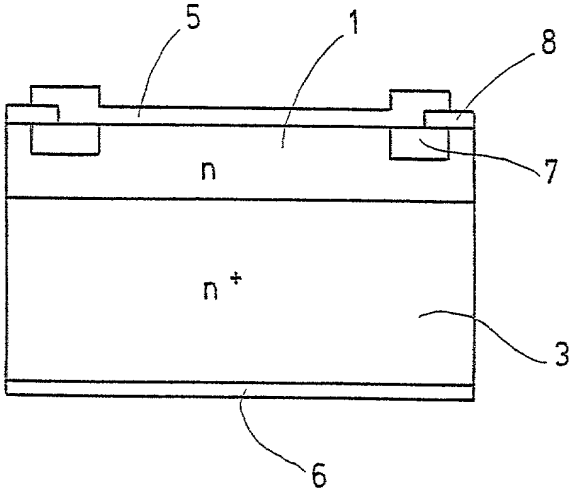

Fig. 5

[10191/2197]

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **DIODE HAVING A METAL SEMICONDUCTOR CONTACT, AND METHOD FOR THE MANUFACTURE THEREOF,** the specification of which was filed as PCT International Application No. **PCT/DE00/01812** on June 3, 2000.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application(s) for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

DE19925050.4 05.06.1999

DE19924510250

PRIOR FOREIGN APPLICATION(S)

Number	Country filed	Day/month/year	Priority Claimed Under 35 USC 119
199 30 781.4	Fed. Rep. of Germany	03 July 1999	Yes

And I hereby appoint Richard L. Mayer (Reg. No. 22,490) and Gerard A. Messina (Reg. No. 35,952) my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful and false statements may jeopardize the validity of the application or any patent issued thereon.

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